# HTS DIPLEXER & LOW NOISE AMPLIFIER RF MODULE

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## ABSTRACT

The design and performance of a 77K, thin film HTS diplexer and low noise amplifier subassembly is described. The diplexer circuit is an all planar design with a 50Ω match at the filter/diplexer manifold interconnect. The low noise amplifier has very low noise figure (0.2 dB) and simultaneously good input/output VSWR when operated at 77K.

## INTRODUCTION

The RF module described below was designed to have a very low input noise figure, 0.5 dB, with 25 MHz wide HTS band pass filters and LNA's in a very small, low mass module. The schematic of the RF circuitry contained in this module is shown in Figure 1. The two RF channels shown in Figure 1 have a common input and separate output connections. The noise figure measured at the RF input of the module is typically 0.5 dB, with 13 dB of gain in each channel. The diplexer is formed using two band pass filters, each with a 50Ω match at the input and output terminals, which are connected together using an HTS diplexer manifold, which also has 50Ω port impedances. The transmission lines used in the manifold are all 50Ω characteristic impedance but with different phase length in order to provide a match over the pass band of the two filters at the input to the diplexer. The advantage of using an all 50 Ω match for the filters and manifold is that the filters can be developed and tested independently of the remaining circuitry.

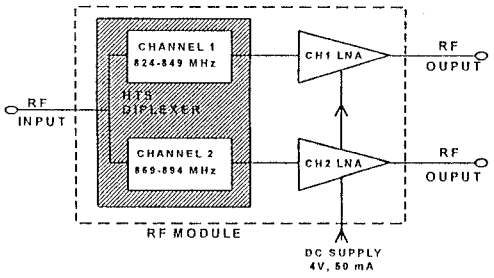


Figure 1. HTS Diplexer/LNA RF module.

The amplifiers are constructed using GaAs FETs, single stages for both channel 1 and channel 2. The amplifiers use two FETs each, in a parallel arrangement to provide a simultaneous noise and conjugate match, with single ended matching structures. The cascaded connection of filters, LNA's and interconnects results in an input noise figure of about 0.5 dB with input and output return losses < 20 dB.

The filters, diplexers and low noise amplifiers are integrated into a miniature RF housing. Figure 2 shows the physical dimensions of the RF Module and the circuits contained within it. Each of the four HTS filters are processed on 1.338" x 0.63" substrates. The module was designed for minimum mass (for fast cool down to 77K) with the whole module weighing 17.3 grams (0.61 oz).

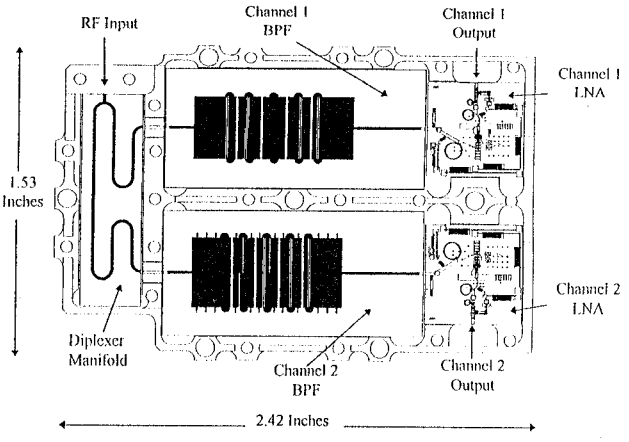


Figure 2. RF Module circuit sizes, physical layout and module design.

## HTS BAND PASS FILTERS

The design of these band-pass filters requires the use of series inductor networks. All other components are either series or shunt capacitors. The filter topology is such that the shunt parasitic capacitances of the inductor networks are absorbed in the capacitive transformation. Figure 3 shows a simple inductor model used in the design of these filters.

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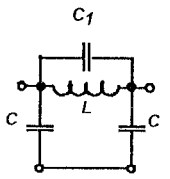



Figure 3. Simple inductor model.

The inductor has some shunt capacitance associated with it that can be modeled as lumped capacitors, $C$ in Figure 3, connected to each end of the inductor, $L$. The inductor model also has a capacitor, $C_1$, connected across the inductor terminals. In order to use this inductor in a filter, a resonator structure must be used that can absorb these capacitors at the ends of the inductor. The inductor model in Figure 3 has been shown to be quite accurate over relatively narrow frequency ranges, thereby allowing for the design of narrow band-pass filters using this model.

A design utilizing these resonators to form lumped element band-pass filters is shown in Figure 4. This filter structure is derived from the generalized equations for the design of band-pass filters from low-pass prototypes as given in [1].

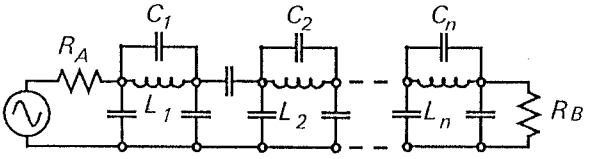



Figure 4. Series inductor lumped element band-pass filter schematic.

The procedure starts with the lumped element low pass prototype of shunt and series connected resonators. The shunt resonators are then replaced by series resonators, with impedance inverters on each end, which yields the basic design for the lumped element band-pass filter with only series resonant elements shown in Figure 5. The design is based upon the reactance slope parameters of the series resonators, $x_j$, and the impedance inverter parameters $K_{n,n+1}$ [1].

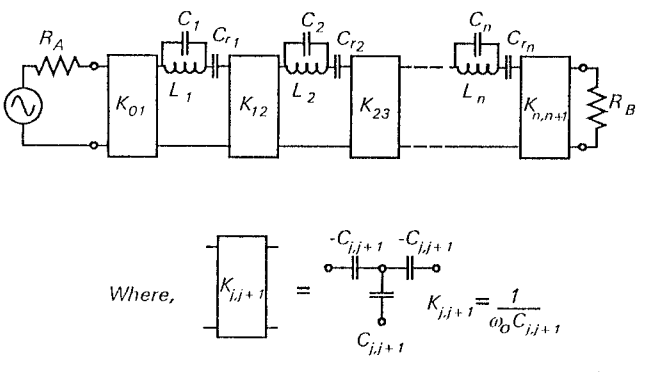
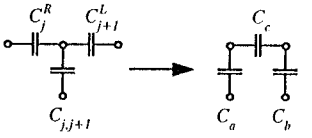



Figure 5. Band-pass filter using series resonators and impedance inverters.

Substituting these relationships into the equations given in [1] yields the filter design with the reactance slope parameters based upon a parallel connection of inductor and capacitor. The next step is to realize the impedance inverters, $K$. In order to have only capacitive shunt elements in the filter design, the $T$-capacitor realization is selected [1]. This has a single shunt capacitor, with two negative capacitors in the series arms of the $T$. Using this form of impedance inverter the negative capacitance can be absorbed in the capacitor used to resonate the parallel connected inductor/capacitor. The capacitor $T$-sections that result can be made symmetrical and can then be converted to $\Pi$ -sections using the well known $T$-$\Pi$ transformation (1), resulting in symmetrical $\Pi$-sections.




$$C_a = \frac{C_j^R C_{j,j+1}}{\sum C}, \quad C_b = \frac{C_{j+1}^L C_{j,j+1}}{\sum C}, \quad C_c = \frac{C_j^R C_{j+1}^L}{\sum C} \qquad (1)$$

$$where, \sum C = C_j^R + C_{j+1}^L + C_{j,j+1}$$

The resulting filter is now very close to the form shown in the Figure 4. The resulting shunt capacitors, $C_a$ and $C_b$, are used to absorb the shunt capacitance from the inductor network. The remaining capacitance can then be realized by adding capacitance to the ends of the inductor network.

The input and output transformers must now be realized. Figure 6 shows a shunt capacitor matching network. The negative series capacitance, $C_{e01}$, can be moved to the other side of the first inductor and absorbed into the inverter. This ultimately results in asymmetric $\Pi$-caps between inductors $L1$ and $L2$ and similarly for inductors $L_{n-1}$ and $L_n$. A benefit of using this type of transformation is that it is done with the minimum number of components (just one) and hence has low sensitivity to inaccuracies in its realization.

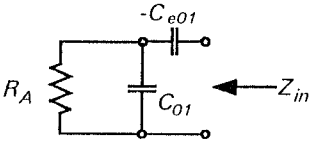



Figure 6. Shunt capacitor matching network.

An in-house linear circuit simulator [2] which runs on an ordinary PC is used to analyze the entire microstrip filter. For the realization of these filters, the capacitor which is connected across the inductor terminals is set to zero. This is done in order to utilize a feature of the in-house linear circuit simulator which gives a matrix of lumped element values which matches the coupled line planar circuit at a single frequency. The filters are manufactured on 0.015" thick MgO using TBCCO.

Quality factors greater than 20,000 are typically measured on resonators. A filter simulation along with its measured response is shown in Figure 7. This is a 5 pole planar thin film HTS Chebyshev bandpass filter with shunt capacitor input and output transformers. It was designed for a VSWR of 1.03:1 and was measured with a VSWR of 1.09:1.

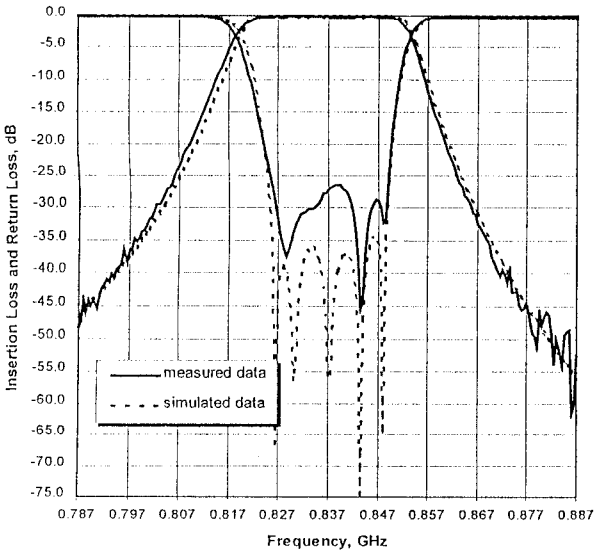



Figure 7. Measured vs. simulated performance of channel 1 band pass filter.

## LOW NOISE AMPLIFIERS

Design of the LNA begins with a careful selection of the active device. For this application simultaneous low noise figure and good input return loss are required. Operation at cryogenic temperature and a desire to minimize the power consumption are also important considerations. A commercially available GaAs HEMT device with a gate width of 280µm and gate length of 0.3µm was selected. This device, connected two in parallel, allows us to achieve simultaneous matching of S11* and Γopt at the desired frequency.

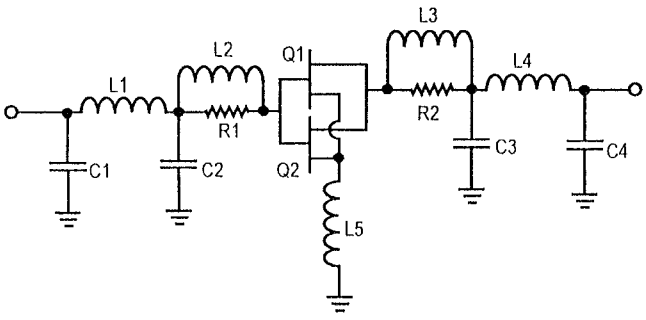



Figure 8. LNA schematic.

Figure 8 shows a schematic representation of the RF circuit for the LNA. The series feedback inductor L5 is chosen to match S11* and Γopt at the desired frequency. Once the conjugate input match is the same as the optimum noise match, the LNA is designed by choosing the values of inductor L1 and capacitors C1 and C2. Since feedback is used in this design, the output matching network (L4, C3 and C4) is also considered during the initial simulation of the LNA to achieve good input and output match with minimum noise figure. Unconditional Stability is achieved without degrading the in-band performance by the selection of L2 and R1 on the input and L3 and R2 on the output. These networks give resistive terminations for the active devices at high frequencies while not adding noise in band.

The entire LNA is cooled to 77K, reducing both the loss of the conductors and the thermal noise generated by that loss and by the stabilization resistors. The LNA is realized on 25 mil thick Alumina using gold conductors. The inductor L5 is realized using gold wire while the other matching components are realized using gold microstrip lines on the alumina substrate. Standard MIC chip and wire techniques modified to allow use in a high vacuum environment are used in the assembly of the LNA.

Figure 9 shows the measured response of a typical LNA. This LNA is tuned for optimum performance at 900 MHz. A gain of approximately 13 dB and input and output return loss of better than 20 dB from 860 MHz to 940 MHz is measured. By adjusting the values of the matching elements (C1, C2, L1 and L5) optimum performance is achieved at any frequency from 840 MHz to 940 MHz. A broadband noise match is also achieved. The measured noise figure for this LNA is approximately 0.20dB across the 850 to 950 MHz band. The LNA is biased at 3.5 Volts drain to source with 25 mA total for the two devices. Even with this low power consumption the LNA with the response shown in figure 9 exhibits an output intercept point of greater than +30 dBm.

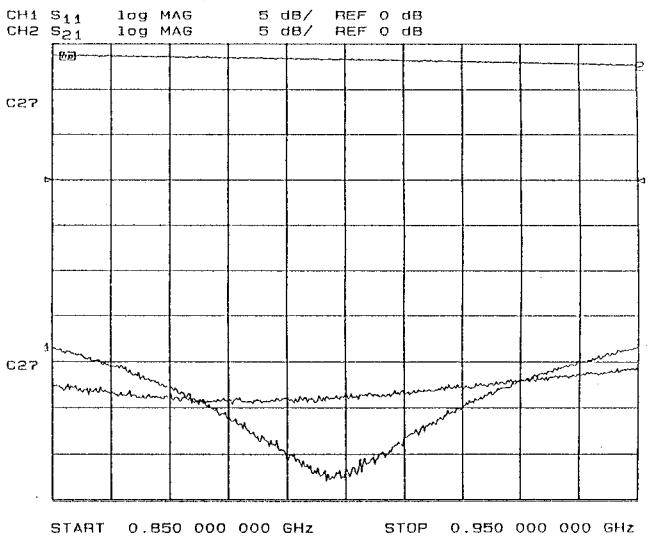



Figure 9. Measured LNA gain, input return loss and output return loss.

## MODULE PERFORMANCE

The diplexer manifold is designed to present 50 Ω terminations at all three ports at the appropriate frequencies. The lengths of the 50 Ω lines are chosen to ensure that at channel 1 frequencies the channel 2 arm presents an open circuit. Also, at the channel 2 frequencies, the channel 1 arm presents an open circuit. By achieving these properties using 50Ω transmission lines, each filter can be easily measured separately before integration.

All of the components are integrated into a single RF module housing as shown in Figure 2. Interconnects are made using gold wire bonds to ohmic contacts on the HTS circuits. The measured performance of the RF module is shown in Figures 10 and 11.

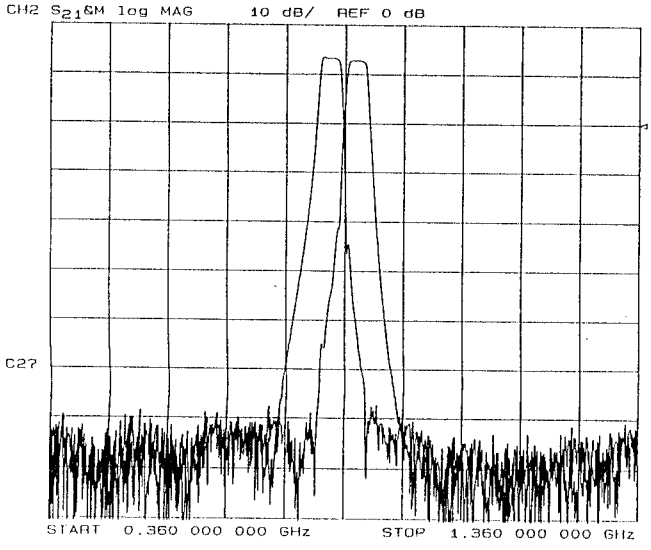



Figure 10. Measured RF module gain and rejection.

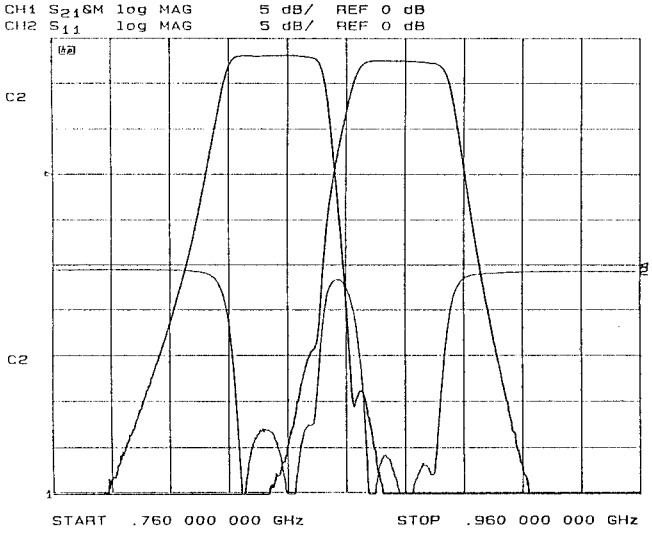



Figure 11. Measured RF module gain and return loss.

Figure 10 shows the measured gain of both paths through the RF module. Each channel has 13 dB of gain and greater than 70 dB of ultimate rejection. Channel 2 is shown to have greater than 20 dB return loss (Figure 11). Figure 12 shows the measured noise figure of the RF module including the loss of an input cryocable (to connect the RF module to the ambient side of a vacuum insulated dewar). Measured noise figure of each channel is less than 0.5 dB.

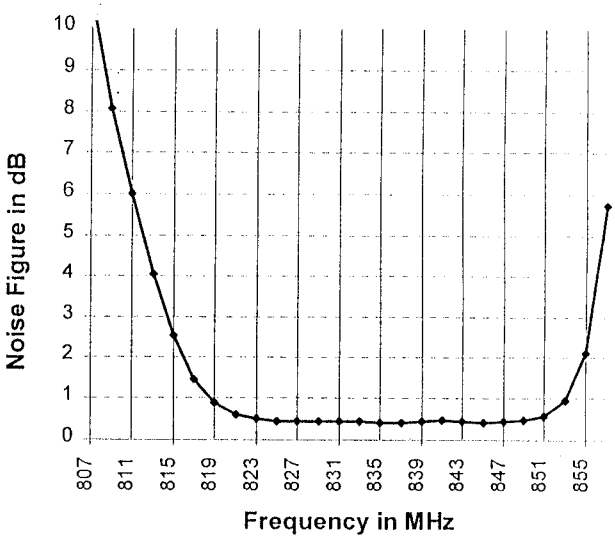



Figure 12. Measured RF module noise figure channel 1.

## ACKNOWLEDGMENTS

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[2] A linear circuit simulation software package developed by Roger Forse at Superconductor Technologies, Inc., Santa Barbara, CA, 93111.